WHAT IS CLAIMED IS:

1. An arbiter circuit comprising:

data transfer request signal holding means for accepting a plurality of data transfer request signals and holding the data transfer request signals in response to predetermined timing signals;

prioritizing means for determining only a signal with the highest priority at a certain point as a valid signal and the signals with lower priorities as invalid signals in order to assign priorities to output signals from the data transfer request signal holding means; and

delaying means for generating data transfer execution signals from the output signals of the prioritizing means.

2. The arbiter circuit according to Claim 1, further comprising a signal delaying means located between the data transfer request signal holding means and the prioritizing means.

3. The arbiter circuit according to Claim 2, wherein the signal delaying means comprises a plurality of stages of inverter circuits connected in series, more stages of the signal delaying means being provided for the data transfer request signals with lower priorities.

4. The arbiter circuit according to Claim 1, wherein the timing signals are generated on the basis of the output

signals of the prioritizing means.

5. The arbiter circuit according to Claim 1, wherein the delaying means is provided for each output signal of the prioritizing means.

6. The arbiter circuit according to Claim 1, wherein the delaying means is provided for the signal recognized as the signal with the highest priority at that point among the output signals of the prioritizing means.

7. The arbiter circuit according to Claim 1, wherein the data transfer request signal holding means comprises a plurality of flip-flop circuits that accepts a plurality of data transfer request signals as input data and has trigger signals (TRE) and reset signals (ARBEND).

8. The arbiter circuit according to Claim 1, wherein the prioritizing means comprises a gate circuit that receives the signals output from the data transfer request signal holding means and the delay signals therefor.

9. The arbiter circuit according to Claim 1, wherein the delaying means comprises a delay circuit to which an even number of stages of delay inverter circuits connected in series is connected, the delay inverter circuits comprising PMOS transistors, resistors and NMOS transistors, and a

circuit that inputs an inversion signal obtained by subjecting an output signal of the prioritizing means to logic inversion to the delay circuit, and takes the logic product of the output signal from the delay circuit associated with the inversion signal, and the inversion signal.

10. The arbiter circuit according to Claim 1, wherein the delaying means comprises a delay circuit having an even number of stages of delay inverter circuits connected in series, the delay inverter circuits comprising PMOS transistors, resistors and NMOS transistors, and generates the data transfer execution signals from the timing signals and the output signals of the prioritizing means.

11. The arbiter circuit according to Claim 10, wherein the delaying means comprises a plurality of delay circuits to which a plurality of stages of delay inverter circuits are connected in series, the delay inverter circuits comprising PMOS transistors, resistors and NMOS transistors, and further comprises means for enabling/disabling the operations of the plurality of delay circuits.